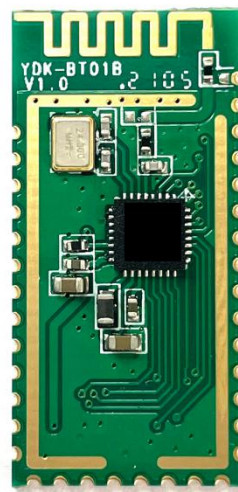


YDK-BT01B

BLE 5.1 Datasheet

Version 1.1



CONTENTS

- 1.INTRODUCTION.....**
- 2. HARDWARE BLOCK DIAGRAM AND PIN DEFINITION.....**
 - 2.1 HARDWARE BLOCK DIAGRAM.....
 - 2.2 PIN DEFINITION.....
- 3.PHYSICAL SIZE.....**
- 4.HARDWARE CIRCUIT INTERFACE.....**
 - 4.1 PIO INTERFACE.....
 - 4.2 IIC INTERFACE.....
 - 4.3 SPI INTERFACE.....
 - 4.4 UART INTERFACE.....
 - 4.5 AUDIO DECODER (OPTIONAL).....
- 5. ELECTRICAL CHARACTERISTICS.....**
 - 5.1 MAXIMUM RATING.....
 - 5.2 RECOMMENDED WORKING CONDITIONS.....
 - 5.3 POWER CONSUMPTION.....
- 6. APPLY REFERENCE CIRCUITS.....**
 - 6.1 MODULE DESIGN REFERENCE CIRCUIT.....
 - 6.2 KEY DESIGN REFERENCE CIRCUIT.....
 - 6.3 LED DESIGN REFERENCE CIRCUIT.....
 - 6.4 LDO BUCK REFERENCE DESIGN CIRCUIT.....

1.Introduction

Overview

YDK-BT01B is a low-power Bluetooth-related product module for SOC (System on Chip) development. It supports 2.4GHz BLE V5.1 protocol. It includes and is fully compatible with Bluetooth V5.0. The module uses Cortex M3 processing. It has powerful computing power. The module also integrates audio codec, PMU (lithium battery charger + LDO), SPI flash ROM with XIP mode, and supports multiple peripherals: IIC, UART, GPIO, ADC, PWM, I2S, SPI, etc. The module has the best power performance, radio frequency performance, stability, versatility and reliability, and is suitable for various application scenarios and different power consumption requirements.

BLE protocol

Bluetooth protocols include L2CAP service layer protocol, security manager protocol (SM), attribute protocol (ATT), general attribute profile protocol (GATT) and general access profile protocol (GAP), etc., including all low energy Bluetooth protocol layers, And supports USB HID man-machine exchange interface, supports multiple connections (1 to 20), and supports mesh related protocols.

Feature

- Comply with Bluetooth specification V5.1 LE
- Transparent transmission rate up to 15kBytes/s
- 150KB ROM,48KB SRAM,Internal 4Mbit Flash
- 32-bit ARM®Cortex®-M3 core processor 48Mhz speed
- The default UART baud rate is 115.2Kbps, which can support 1200bps to 921.6Kbps
- Integrated DC-DC regulator
- Mono audio codec (optional)
- Maximum Tx power up to +10dBm
- Low power , serial port and APP wake up
- Support master-slave integration and multiple connections
- Supports up to two UARTs and 17 reusable GPIOs
- IIC interface, support external EEPROM or IIC sensor

- Support up to 4 channels of 10-bit ADC voltage acquisition

Peripherals

- GPIO
- UART
- SPI
- I2C
- I2S
- PWM
- ADC
- LED

Application



Figure 1 Application

- Bluetooth light control
- Low Energy Bluetooth Smart Lock
- IoT BLE sensor network
- Smart home
- Bluetooth POS machine
- Handheld PTZ camera
- HID remote control
- Voice remote control
- iBeacon
- Electronic medical equipment

PIN	PIN NAME	TYPE	Pin description	Comment
1	UART_TX	I/O	UART output	
2	UART_RX	I/O	UART input	
3	PIO0	I/O	Programmable reusable input/output	
4	PIO1	I/O	Programmable reusable input/output	
5	NC		NC	
6	NC		NC	
7	NC		NC	
8	NC		NC	
10	NC		NC	
11	RESET	I	Hardware reset (please leave it open if not needed)	
12	VCC	VDD	Power supply voltage 1.8V to 4.3V (recommended 3.3V)	
13	GND	VSS	ground	
14	GND	VSS	ground	
15	Data	I/O	Burn port	
16	Clock	O	Burn port	
17	NC		NC	
18	NC		NC	
19	NC		NC	
20	NC		NC	
21	GND	VSS	ground	
22	GND	VSS	ground	
23	PIO2	I/O	Programmable reusable input/output (Used as a button by default)	1
24	PIO3	I/O	Programmable reusable input/output	
25	PIO4	I/O	Programmable reusable input/output	
26	NC		NC	
27	NC		NC	
28	PIO5	I/O	Programmable reusable input/output	
29	PIO6	I/O	Programmable reusable input/output	
30	PIO7	I/O	Programmable reusable input/output	
31	PIO8	I/O	Programmable reusable input/output	
32	PIO9	I/O	Programmable reusable input/output (used as Bluetooth receiving data indication default)	2
33	LED	I/O	Used as a Bluetooth work indicator	3
34	PIO10	I/O	Programmable reusable input/output (Used as Bluetooth connection status indicator default)	4
35	GND	VSS	External antenna RF ground	
36	EXT_ANT	O	External antenna RF signal output	

Module pin notes:

Comment 1 Disconnect the Bluetooth connection (default). In the Bluetooth connection state, input a low-level pulse to this pin to disconnect the Bluetooth connection.

Comment 2	Bluetooth receiving data indicator (default)-Power on: pull down; receive APP data: pull up 10ms
Comment 3	Bluetooth working indicator (default)-Power on: the indicator flashes slowly; Connected: pulls high and keeps on.
Comment 4	Bluetooth connection status (default)-Power on: pull down; Connected: pull up and keep on, disconnect Bluetooth connection: pull down.

3.Physical size

- Module nominal size: 13.0mm(W) x 26.9mm(L) x 0.6 mm(H) Tolerance: ±0.2mm
- Module size: 13.0mm X 26.9mm Tolerance: ±0.1mm
- Land size: 0.8mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.1mm Tolerance: ±0.1mm

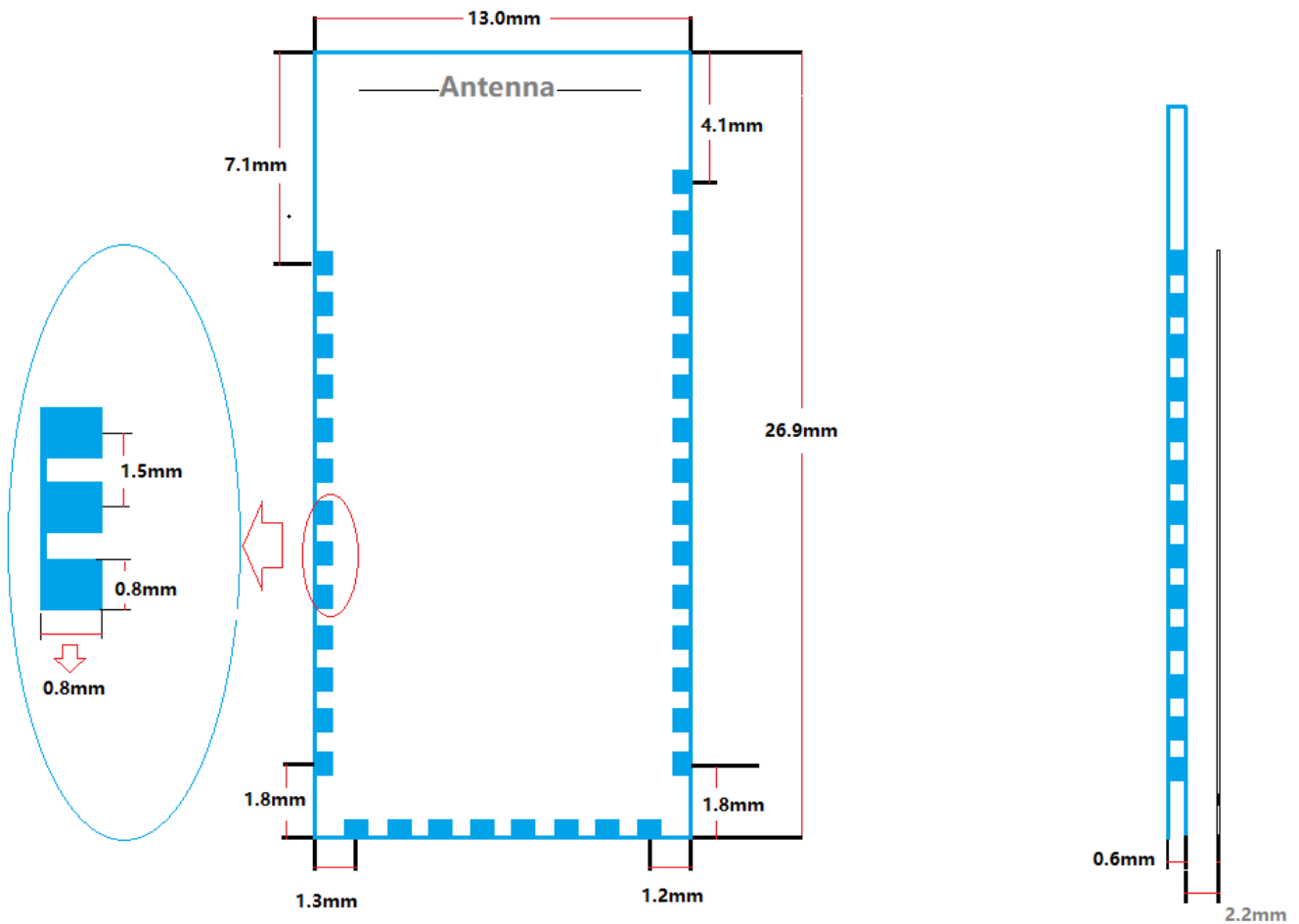


Figure 4 Physical dimensions

4.Hardware circuit interface

4.1 PIO interface

The module defines 4 general-purpose digital IOs by default, which can be multiplexed into four 10-bit precision ADC interfaces for the user's ADC sampling voltage requirements. Such as external ADC sensor voltage collection.

PIN	PIN NAME	TYPE	Pin description	Comment
-----	----------	------	-----------------	---------

1	UART_TX	I/O	Default output	UART data	SDA0/I2SFRM/PWM5/SSPCSN/UTXD0/UTXD1/ANTCTL0/PDMDAT/PWM4/ADC1
2	UART_RX	I/O	Default input	UART data	SCL0/I2SCLK/PWM4/SSPCLK/URXD0/URXD1/ANTCTL0/PDMCLK/PWM5/ADC0
3	PIO0	I/O	Programmable reusable input/output		SDA1/I2SDIN/PWM1/SSPDIN/UTXD0/UTXD1/ANTCTL1/PDMDAT/PWM0/ADC3
4	PIO1	I/O	Programmable reusable input/output		SDA1/I2SDIN/PWM5/SSPDIN/UTXD0/UTXD1/SWDIO/PDMDAT/PWM4
15	Data	I/O	Default burning port		SCL1/I2SDOUT/PWM2/SSPDOUT/URXD0/URXD1/ANTCTL0/PDMCLK/PWM3
16	Clock	I/O	Default burning port		SDA1/I2SDIN/PWM3/SSPDIN/UTXD0/UTXD1/ANTCTL1/PDMDAT/PWM2
23	PIO2	I/O	Programmable reusable input/output		SCL1/I2SDOUT/PWM0/SSPDOUT/URXD0/URXD1/CLKOUT/PDMCLK/PWM1/ADC2
24	PIO3	I/O	Programmable reusable input/output		SCL1/I2SDOUT/PWM4/SSPDOUT/URXD0/URXD1/SWTCK/PDMCLK/PWM5
25	PIO4	I/O	Programmable reusable input/output		SDA0/I2SFRM/PWM5/SSPCSN/UTXD0/UTXD1/SWV/PDMDAT/PWM4
28	PIO5	I/O	Programmable reusable input/output		SDA0/I2SFRM/PWM5/SSPCSN/UTXD0/UTXD1/ANTCTL1/PDMDAT/PWM4
29	PIO6	I/O	Programmable reusable input/output		SCL0/I2SCLK/PWM0/SSPCLK/URXD0/URXD1/CLKOUT/PDMCLK/PWM1
30	PIO7	I/O	Programmable reusable input/output		SDA1/I2SDIN/PWM1/SSPDIN/UTXD0/UTXD1/ANTCTL0/PDMDAT/PWM0
31	PIO8	I/O	Programmable reusable input/output		SCL1/I2SDOUT/PWM0/SSPDOUT/URXD0/URXD1/CLKOUT/PDMCLK/PWM1
32	PIO9	I/O	Programmable reusable input/output		SCL0/I2SCLK/PWM4/SSPCLK/URXD0/URXD1/CLKOUT/PDMCLK/PWM5
34	PIO10	I/O	Programmable reusable input/output		SDA0/I2SFRM/PWM1/SSPCSN/UTXD0/UTXD1/ANTCTL0/PDMDAT/PWM0

Table 4.1 PIO multiplexing table

4.2 IIC interface

The module supports IIC bus communication, a serial interface composed of two lines of SDA and SCL data clocks, supports two modes of standard IIC communication and fast IIC communication, and can customize multiple clock rates. The IIC write timing diagram is as follows:

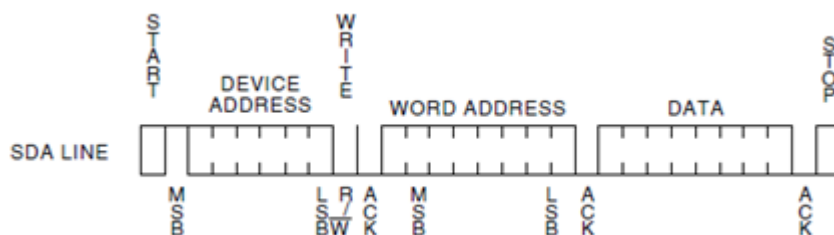


Figure 5 IIC write timing diagram

Note: All PIOs can be reused as IIC SDA and IIC SCL. For details, please refer to Table 4.1 PIO Multiplexing Table.

4.3 SPI interface

- ⊙ Support SPI communication with faster full-duplex data transmission rate
- ⊙ SDO/MOSI-master device data output, slave device data input
- ⊙ SDI/MISO-master device data input, slave device data output
- ⊙ SCLK-clock signal, generated by the master device
- ⊙ CS/SS-slave device enable signal, controlled by the master device. When there are multiple slave devices, because each slave device has a chip select pin connected to the master device, when our master device communicates with a slave device, the corresponding chip of the slave device will be required. Select the pin level to be pulled low or pulled high

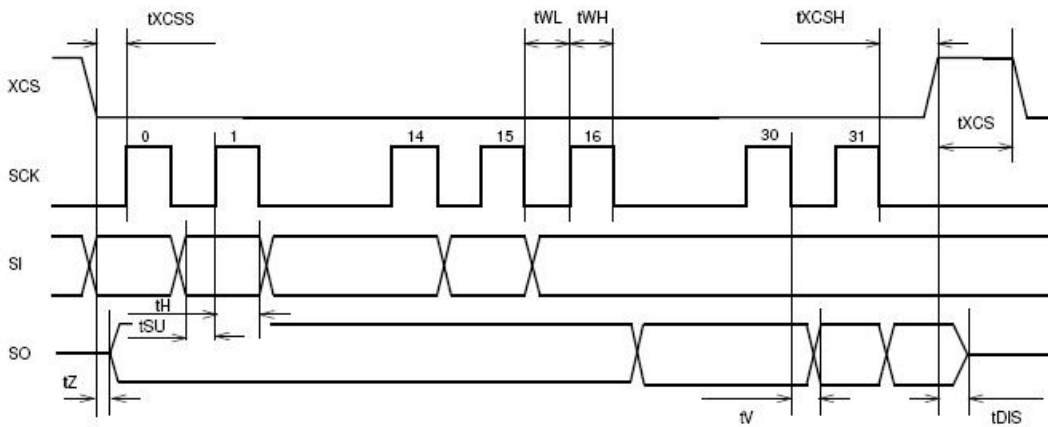


Figure 6 SPI timing diagram

4.4 UART interface

The module supports up to two UARTs. By default, only one is enabled for customer use. The serial port baud rate supports 1200bps~921600bps, and the default (115200, 8, N, 1). There is a FIFO buffer mechanism for serial data reception, and the default maximum buffer size is 2k Bytes, which can prevent data loss. The default CTS and RTS are invalid. The peripheral MCU communicates with YDK-BT01B module UART, and the simple reference connection circuit is shown in Figure 4. .

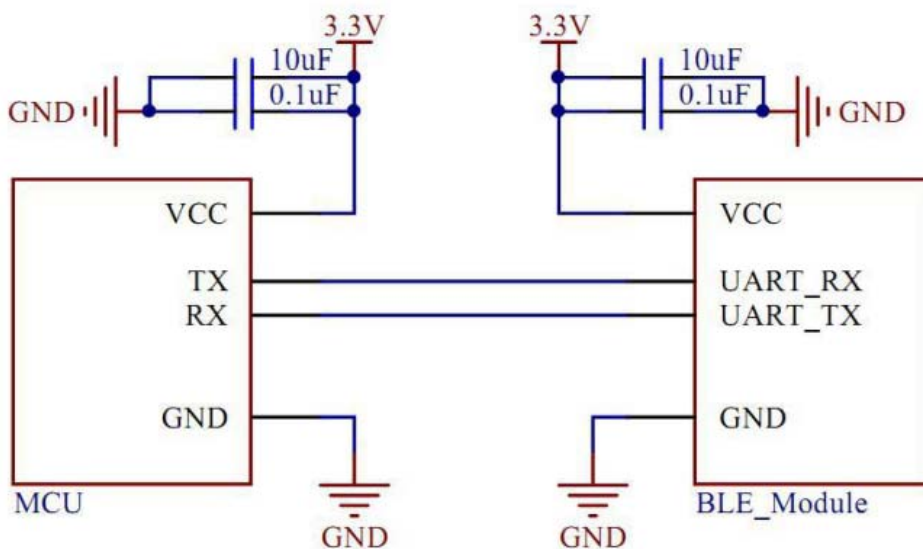


Figure 7 Simple connection reference circuit

4.5 Audio decoder (optional)

Simpler hardware circuit realization, users only need external amplifier circuit to realize audio playback or MIC input

- ✚ Single channel 16bit Σ ADC
- ✚ 32-byte depth of FIFO received and sent
- ✚ Into PGA -17.25 db-30db gain
- ✚ DAC/ADC supports 8k/16k/44.1k/48kHz sampling rate (up to 48khz)

For more parameters, see the following table 4.5 Audio Decoding Parameter Table

parameter	Minimum	Max	unit
Sampling Rate	8	48	KHZ
Digital gain	-48	32	dB
Analog gain	0	30	dB
DAC output voltage (VDD 2.9V=average 1500)			mv

Table 4.5 Audio decoding parameter table

5. Electrical characteristics

5.1 Maximum rating

The absolute maximum ratings of the power supply voltage on the digital and analog pins of the module are listed below. Continuous operation under these conditions or above may permanently damage the equipment.

parameter	Minimum	Max	unit
Core supply voltage	0.9	1.3	V
Input/output voltage	1.6	3.3	V
Supply voltageVBAT	1.8	4.3	V
Supply voltageVCHG	4.75	5.25	V
Storage temperature	-40	125	°C
Operating temperature	-40	80	°C

Table 5.1 Maximum ratings

5.2 Recommended working conditions

Recommended working conditions parameters	Minimum	Typ	Max	unit
Core supply voltage	0.9	1.2	+1.3	V
Input/output voltage	1.6	2.9	3.3	V
Supply voltageVBAT	1.8	3.3	4.3	V
Supply voltageVCHG	4.75	5	5.25	V
Storage temperature	-40	20	125	°C
Operating temperature	-40	20	80	°C

Table 5.2 Recommended working conditions

5.3 Power consumption

Operating mode	Average	Max	unit
Tx Peak current (0dB)		8	mA
Rx Peak current (0dB)		9.7	mA
Deep sleep current	6.1		μ A
Power off	2.7		μ A

Table 5.3 Power consumption

6. Apply reference circuits

6.1 Module design reference circuit

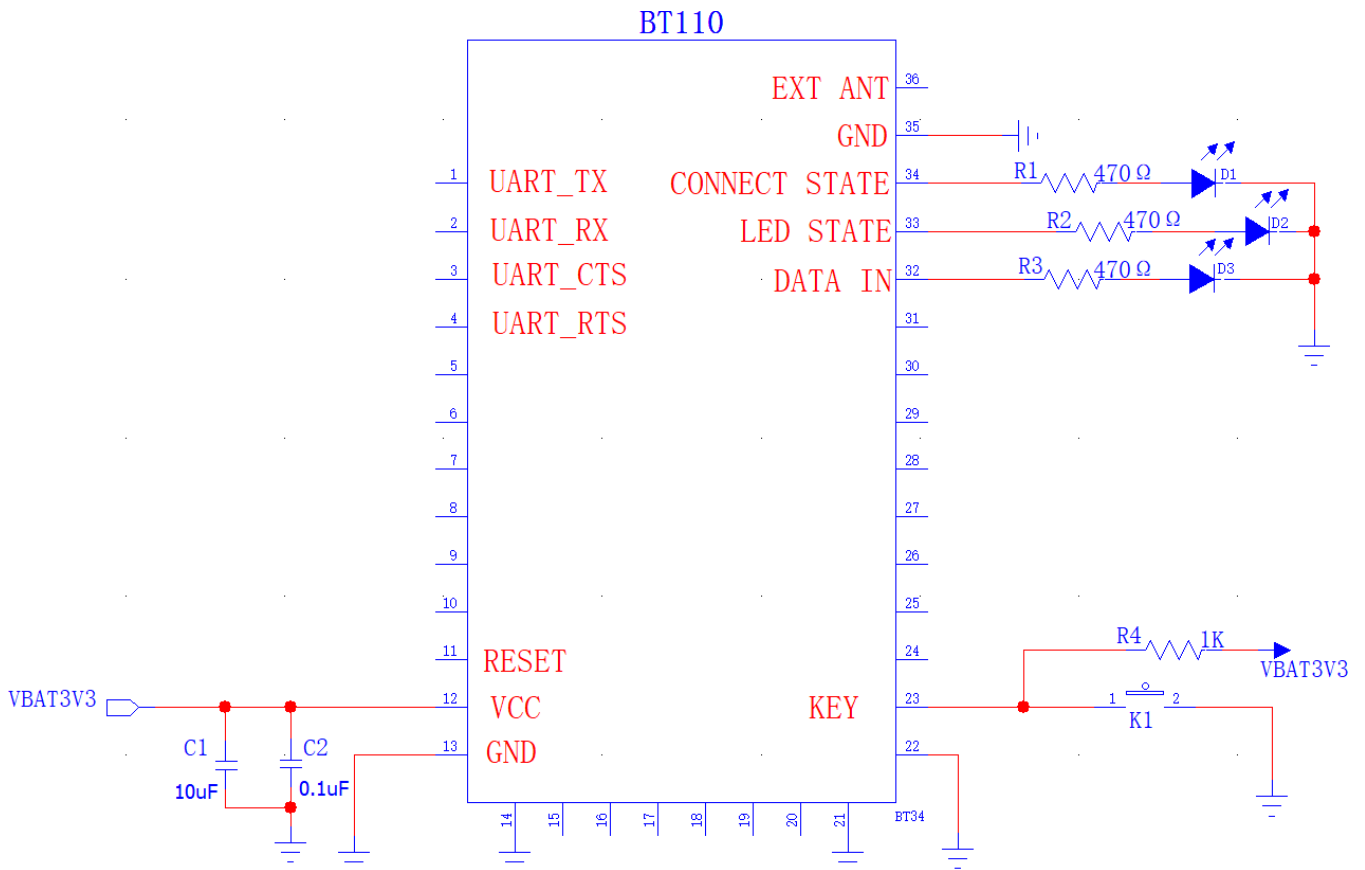


Figure 8 Reference circuit for module design

6.2 Key design reference circuit

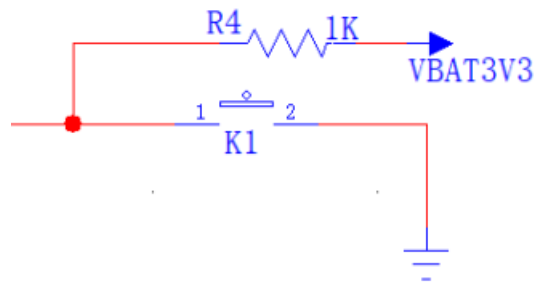


Figure 9 Button reference

6.3 LED design reference circuit

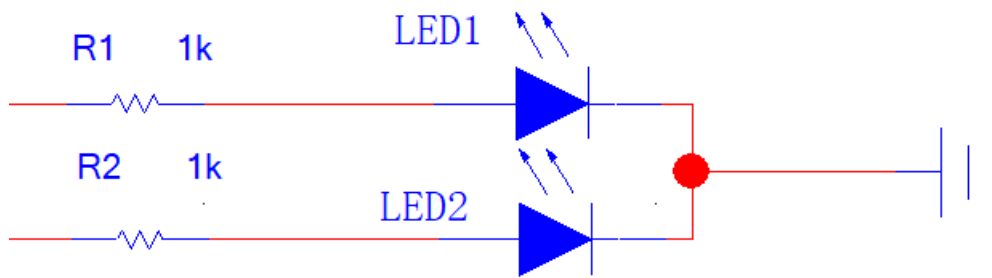


Figure 10 LED reference

6.4 LDO buck reference design circuit

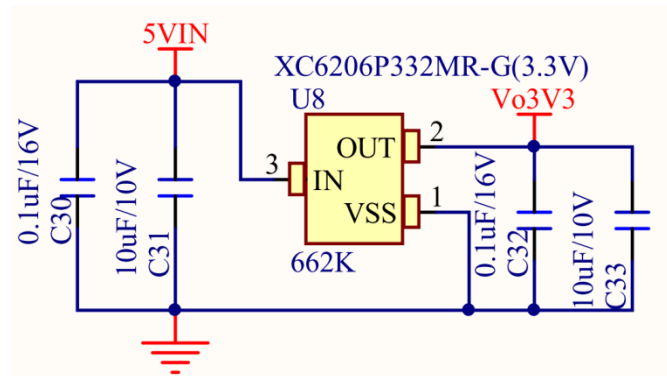


Figure 11 LDO buck reference