# YDK-BT01S

## BLE 5.1 Datasheet

## Version 1.2

# Revision record

| version | date | recording | Author |
|---|---|---|---|
| 1.0 | 2021/01/01 | First Release | Vasily |
| 1.1 | 2021/01/05 | Add function overview, PIN description, modify reference circuit | Richard |
| 1.2 | 2021/01/10 | Modify block diagram, size diagram, add PIO description | Vasily |
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目录



# 1.Introduction

## Overview

YDK-BT01S is a low-power Bluetooth-related product module for SOC (System on Chip) development. It supports 2.4GHz BLE V5.1 protocol. It includes and is fully compatible with Bluetooth V5.0. The module uses Cortex M3 processing. Supports multiple peripherals: IIC, UART, GPIO, ADC, PWM, SPI, etc. The module has the best power performance, radio frequency performance, stability, versatility and reliability, and is suitable for various application scenarios and different power consumption requirements.

## BLE protocol

Bluetooth protocols include L2CAP service layer protocol, security manager protocol (SM), attribute protocol (ATT), general attribute profile protocol (GATT) and general access profile protocol (GAP), etc., including all low energy Bluetooth protocol layers , And supports USB HID man-machine exchange interface, supports multiple connections, and supports mesh related protocols.

## Feature

- Comply with Bluetooth specification V5.1 LE
- Transparent transmission rate up to 15kBytes/s
- 150KB ROM,48KB SRAM,Internal 4Mbit Flash
- 32-bit ARM®Cortex®-M3 core processor 48Mhz speed
- The default UART baud rate is 115.2Kbps, which can support 1200bps to 921.6Kbps
- Integrated DC-DC regulator
- Maximum Tx power up to +10dBm
- Low power , serial port and APP wake up
- Support master-slave integration and multiple connections
- Supports up to two UARTs and 7 reusable GPIOs
- IIC interface, support external EEPROM or IIC sensor
- Support up to 3 channels of 10-bit ADC voltage acquisition

## Peripherals

- GPIO
- UART
- SPI
- I2C
- PWM
- ADC

## Application


Figure 1 Application

- Bluetooth light control
- Low Energy Bluetooth Smart Lock
- IoT BLE sensor network
- Smart home
- Bluetooth POS machine
- Handheld PTZ camera
- HID remote control
- iBeacon
- Electronic medical equipment

# 2. Hardware block diagram and pin definition

## 2.1 Hardware block diagram

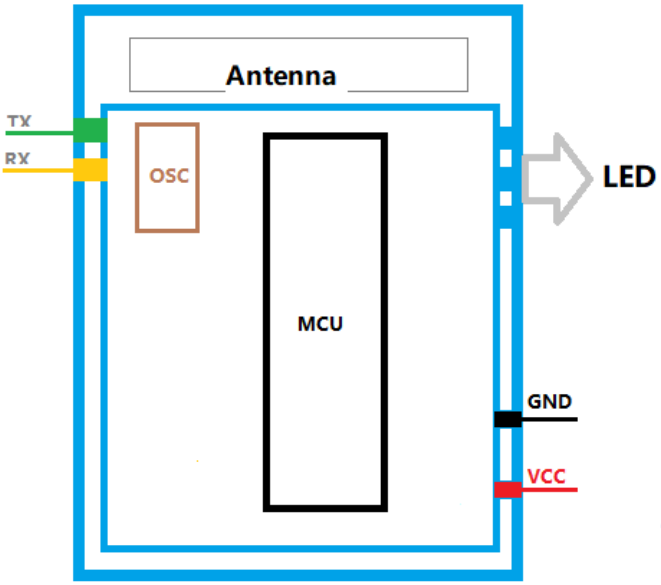


Figure 2 Block diagram

## 2.2 Pin definition

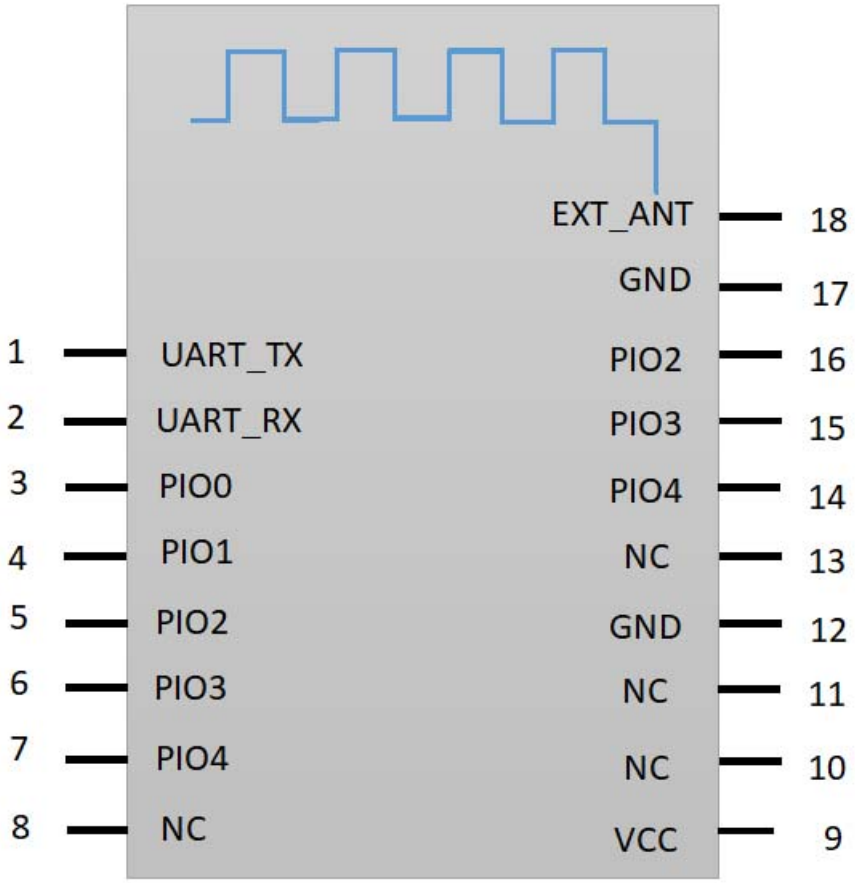


图 3 YDK-BT01S pin definition

| PIN | PIN NAME | TYPE | Pin description | Comment |
|---|---|---|---|---|
| 1 | UART_TX | O | UART output | |
| 2 | UART_RX | I | UART input | |
| 3 | PIO0 | I/O | Programmable reusable input/output | |
| 4 | PIO1 | I | Programmable reusable input/output | |
| 5 | PIO2 | | Programmable reusable input/output | |
| 6 | PIO3 | | Programmable reusable input/output | |
| 7 | PIO4 | | Programmable reusable input/output | |
| 8 | NC | | NC | |
| 9 | VCC | VDD | Power supply voltage 1.8V to 4.3V (recommended 3.3V) | |
| 10 | NC | | NC | |
| 11 | NC | | NC | |
| 12 | GND | VSS | ground | |
| 13 | NC | | NC | |
| 14 | PIO4 | I/O | Programmable reusable input/output | 1 |
| 15 | PIO3 | I/O | Programmable reusable input/output | 2 |
| 16 | PIO2 | I/O | Programmable reusable input/output | 3 |

| | | | |
|---|---|---|---|
| 17 | GND | VSS | External antenna RF ground |
| 18 | EXT_ANT | O | External antenna RF signal output |

Comments:

| | |
|---|---|
| **Comment** 1 | Bluetooth connection status (default)-Power on: pull down; Connected: pull up and keep on, disconnect Bluetooth connection: pull down. |
| **Comment** 2 | Bluetooth working indicator (default)-Power on: the indicator flashes slowly; Connected: pulls high and keeps on. |
| **Comment** 3 | Disconnect the Bluetooth connection (default). In the Bluetooth connection state, input a low-level pulse to this pin to disconnect the Bluetooth connection. |

# 3.Physical size

- Module nominal size: 16.1mm(W) x 19.8mm(L) x 0.6 mm(H) Tolerance: ±0.2mm
- Module size: 16.1mm X 19.8mm Tolerance: ±0.1mm
- Land size: 0.9mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.1mm Tolerance: ±0.1mm

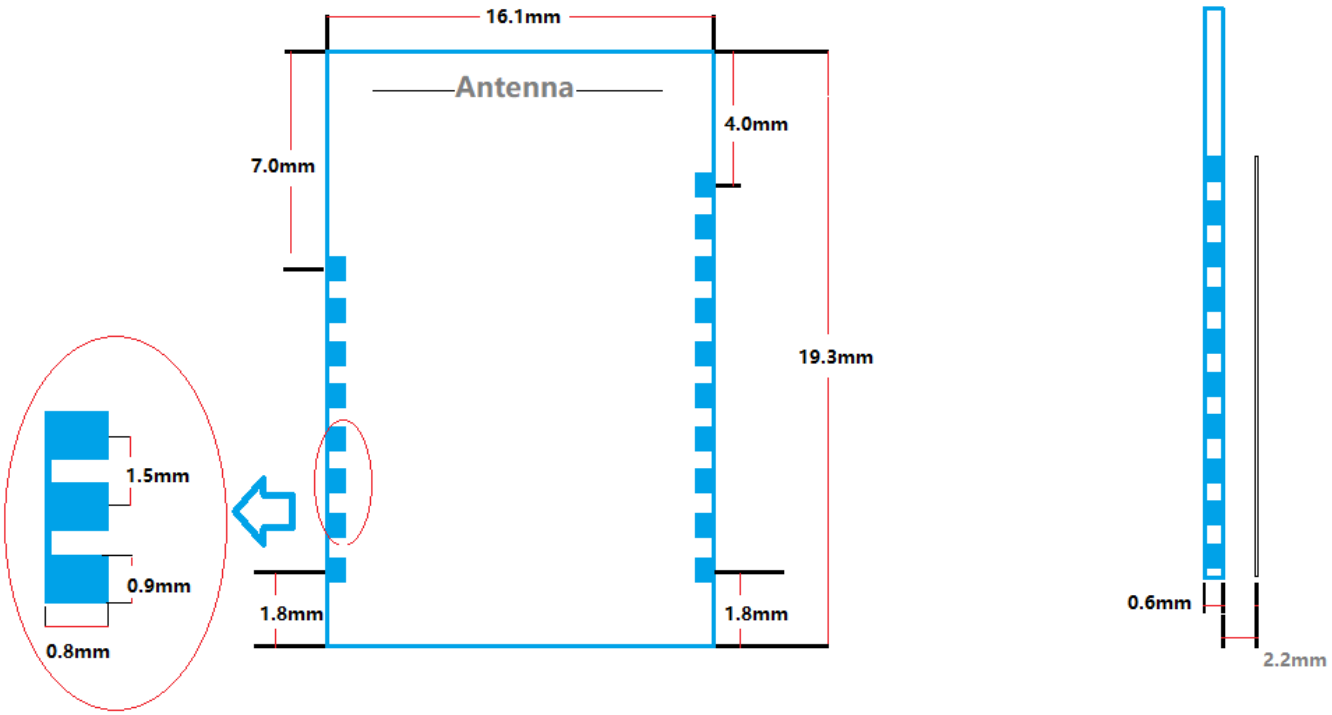


Figure 4 Physical dimensions

# 4.Hardware circuit interface

## 4.1 PIO interface

The module defines 3 general-purpose digital IOs by default, which can be multiplexed into four 10-bit precision ADC interfaces for the user's ADC sampling voltage requirements. Such as external ADC sensor voltage collection.

| PIN | PIN NAME | TYPE | Pin description | Comment |
|---|---|---|---|---|
| 1 | UART_TX | I/O | Default UART data output | SDA1/PWM5/SSPDIN/UTXD0/UTXD1/SWDIO/PDMDAT/PWM4 |

| | | | | |
|---|---|---|---|---|
| 2 | UART_RX | I/O | Default UART data input | SCL1/PWM4/SSPDOUT/URXD0/URXD1/SWTCK/PDMCLK/PWM5 |
| 3 | PIO0 | I/O | Default burning port | SDA1/PWM3/SSPDIN/UTXD0/UTXD1/ANTCTL1/PDMDAT/PWM2 |
| 4 | PIO1 | I/O | Default burning port | SCL1/PWM2/SSPDOUT/URXD0/URXD1/ANTCTL0/PDMCLK/PWM3 |
| 5,16 | PIO2 | I/O | Programmable reusable input/output | SCL1/PWM0/SSPDOUT/URXD0/URXD1/CLKOUT/PDMCLK/PWM1/ADC2 |
| 6,15 | PIO3 | I/O | Programmable reusable input/output | SDA0/PWM5/SSPCSN/UTXD0/UTXD1/ANTCTL0/PDMDAT/PWM4/ADC1 |
| 7,14 | PIO4 | I/O | Programmable reusable input/output | SCL0/PWM4/SSPCLK/URXD0/URXD1/ANTCTL0/PDMCLK/PWM5/ADC0 |

Table 4.1 PIO multiplexing table

## 4.2 IIC interface

The module supports IIC bus communication, a serial interface composed of two lines of SDA and SCL data clocks, supports two modes of standard IIC communication and fast IIC communication, and can customize multiple clock rates. The IIC write timing diagram is as follows:

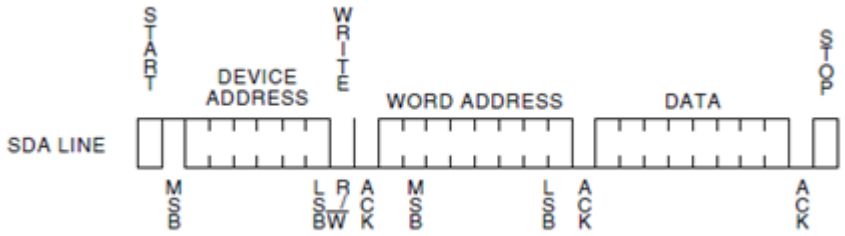


Figure 5 IIC write timing diagram

Note: All PIOs can be reused as IIC SDA and IIC SCL. For details, please refer to Table 4.1 PIO Multiplexing Table.

## 4.3 SPI interface

- Support SPI communication with faster full-duplex data transmission rate
- SDO/MOSI-master device data output, slave device data input
- SDI/MISO-master device data input, slave device data output
- SCLK-clock signal, generated by the master device
- CS/SS-slave device enable signal, controlled by the master device. When there are multiple slave devices, because each slave device has a chip select pin connected to the master device, when our master device communicates with a slave device, the corresponding chip of the slave device will be required. Select the pin level to be pulled low or pulled high

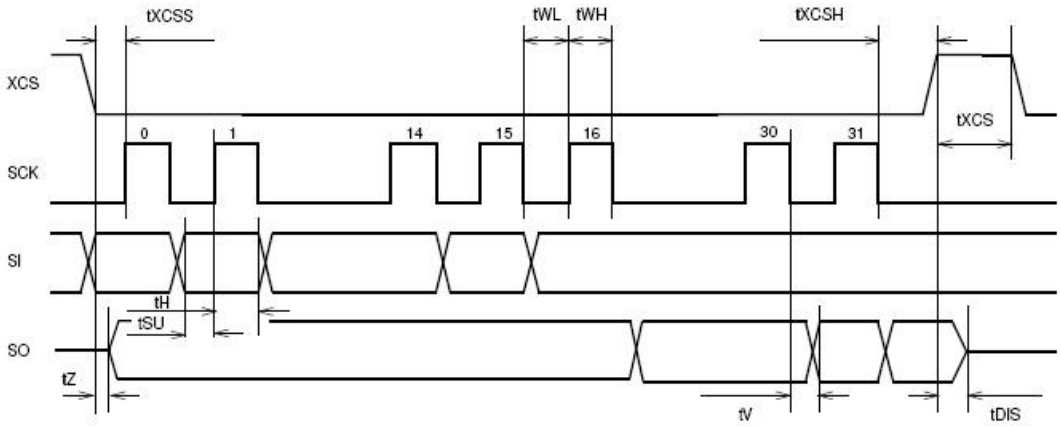


Figure 6 SPI timing diagram

## 4.4 UART interface

The module supports up to two UARTs. By default, only one is enabled for customer use. The serial port baud rate supports 1200bps~921600bps, and the default (115200, 8, N, 1). There is a FIFO buffer mechanism for serial data reception, and the default maximum buffer size is 2k Bytes, which can prevent data loss. The default CTS and RTS are invalid. The peripheral MCU communicates with YDK-BT01S module UART, and the simple reference connection circuit is shown in Figure 4.。

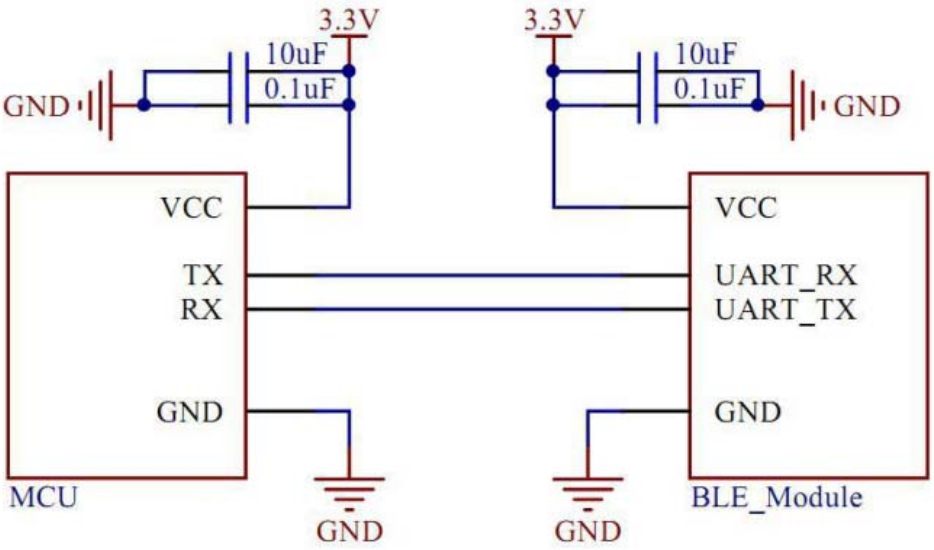


Figure 7 Simple connection reference circuit

# 5. Electrical characteristics

## 5.1 Maximum rating

The absolute maximum ratings of the power supply voltage on the digital and analog pins of the module are listed below. Continuous operation under these conditions or above may permanently damage the equipment.

| parameter | Minimum | Max | unit |
|---|---|---|---|
| Core supply voltage | 0.9 | 1.3 | V |
| Input/output voltage | 1.6 | 3.3 | V |

| | | | |
|---|---|---|---|
| Supply voltageVBAT | 1.8 | 4.3 | V |
| Supply voltageVCHG | 4.75 | 5.25 | V |
| Storage temperature | -40 | 125 | ℃ |
| Operating temperature | -40 | 80 | ℃ |

Table 5.1 Maximum ratings

## 5.2 Recommended working conditions

| Recommended working conditions parameters | Minimum | Typ | Max | unit |
|---|---|---|---|---|
| Core supply voltage | 0.9 | 1.2 | +1.3 | V |
| Input/output voltage | 1.6 | 2.9 | 3.3 | V |
| Supply voltageVBAT | 1.8 | 3.3 | 4.3 | V |
| Supply voltageVCHG | 4.75 | 5 | 5.25 | V |
| Storage temperature | -40 | 20 | 125 | ℃ |
| Operating temperature | -40 | 20 | 80 | ℃ |

Table 5.2 Recommended working conditions

## 5.3 Power consumption

| Operating mode | Average | Max | unit |
|---|---|---|---|
| Tx Peak current（0dB） | | 8 | mA |
| Rx Peak current（0dB） | | 9.7 | mA |
| Deep sleep current | 6.1 | | μA |
| Power off | 2.7 | | μA |

Table 5.3 Power consumption

# 6. Apply reference circuits

## 6.1 Module design reference circuit

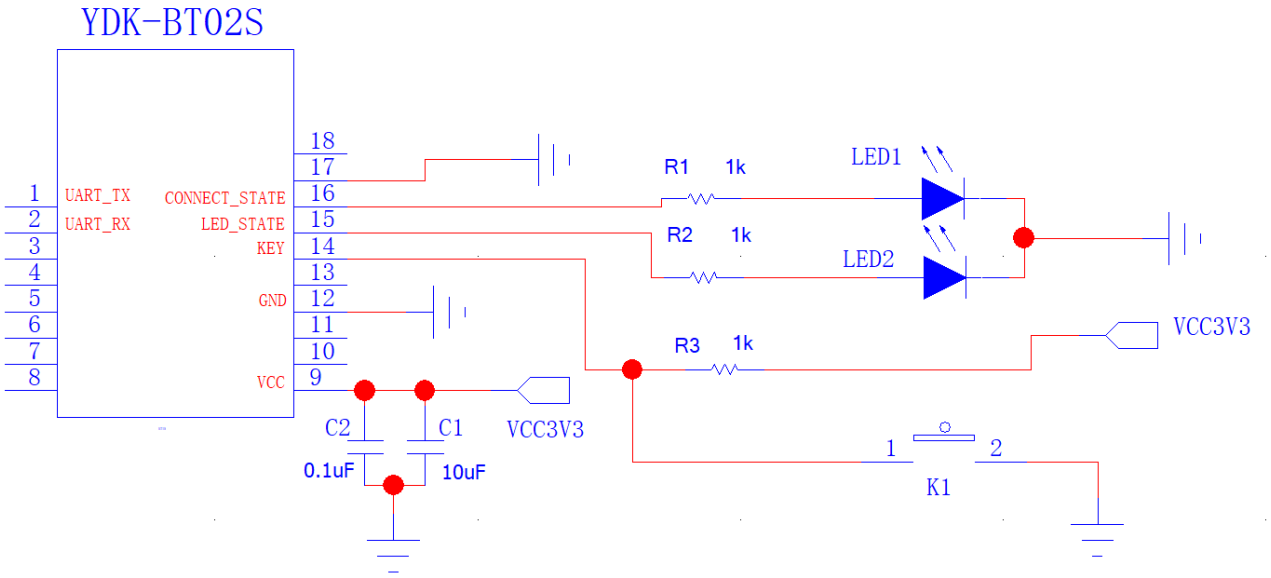


Figure 8 Reference circuit for module design

## 6.2 Key design reference circuit

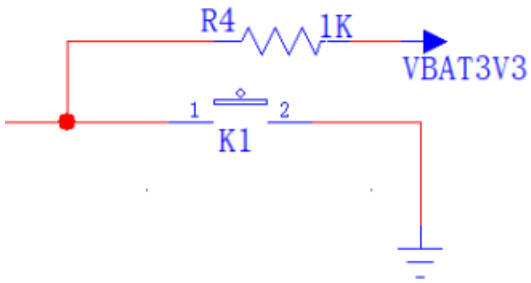


Figure 9 Button reference

## 6.3 LED design reference circuit

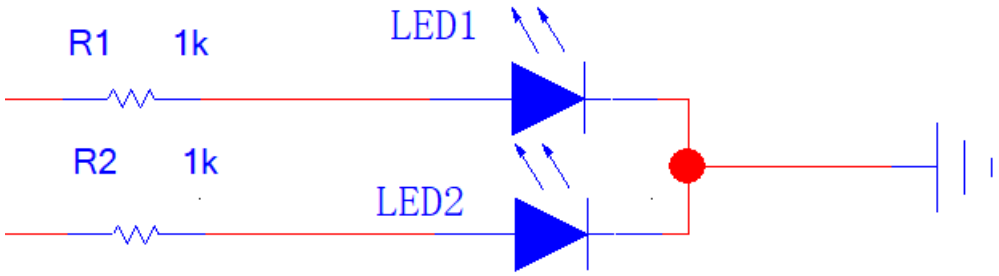


Figure 10 LED reference

## 6.4 LDO buck reference design circuit

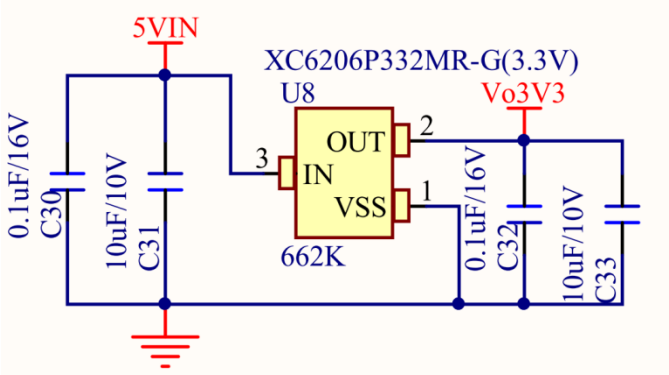


Figure 11 LDO buck reference